Fraunhofer MIKROELEKTRONIK

Forschungsfabrik Mikroelektronik Deutschland

Fraunhofer Group for Microelectronics in Cooperation with the Leibniz Institutes FBH and IHP

PRESS RELEASE

European Chiplet Innovation: APECS Pilot Line starts Operation in the Framework of the EU Chips Act

The pilot line for "Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems" (APECS) marks a major leap forward in strengthening Europe's semiconductor manufacturing capabilities and chiplet innovation as part of the EU Chips Act. By providing large industry players, SMEs, and start-ups with a facilitated access to cutting-edge technology, the *APECS* pilot line will establish a strong foundation for resilient and robust European semiconductor supply chains. Within *APECS,* the institutes collaborating in the Research Fab Microelectronics Germany (FMD) will work closely with European partners, to make a significant contribution to the European Union´s goals of increasing technological resilience, strengthening cross-border collaboration and enhancing its global competitiveness in semiconductor technologies. APECS is co-funded by the Chips Joint Undertaking and national funding authorities of Austria, Belgium, Finland, France, Germany, Greece, Portugal, Spain, through the "Chips for Europe" initiative. The overall funding for APECS amounts to € 730 million over 4.5 years.

Europe is home to a vibrant ecosystem of (hidden) champions, from traditional enterprises in vertical markets, to SMEs and start-ups the competitive advantages of which lie in superior semiconductor-based solutions. Nevertheless, many of these companies are currently confronted with limited access to advanced semiconductor technologies, while at the same time these technologies are increasingly becoming the most important factor for innovation and market growth.

The European Commission is investing significant resources under the EU Chips Act to strengthen semiconductor technologies and applications in the European Union. This aims to enhance Europe's technological resilience, secure supply and value chains, and drive innovation in emerging fields such as energy efficient AI, manufacturing, mobility, information and communications, neuromorphic and quantum computing as well as trusted and sustainable electronics.

The *APECS* pilot line focuses on bridging application-oriented research with innovative developments in heterogeneous integration*, in particular emerging chiplet** technologies. By pushing beyond conventional system-in-package (SiP) methods, *APECS* will deliver robust and trusted heterogeneous systems, significantly boosting the innovation capacity of the European semiconductor industry.

Investments in strategic projects such as *APECS* under the EU Chips Act, is crucial for positioning Europe as an indispensable partner in the global technology sector. Germany plays a key role in this endeavor – both as a leading research hub and a driving economic force. Thanks to substantial funding from the German Federal Ministry of Education and Research (BMBF) and the federal states of Saxony, Berlin, Bavaria, Schleswig-Holstein, Baden-Württemberg, North Rhine-Westphalia, Brandenburg, and Saxony-Anhalt, it will be possible to further expand the R&D infrastructure in the coming years within the framework of the APECS pilot line. This represents a crucial step toward ensuring the long-term economic stability of both Germany and Europe.

"Fraunhofer plays a central role in the implementation of major projects such as APECS, which strengthen Germany's technological resilience and capacity for innovation," emphasizes Prof. Holger Hanselka, President of the Fraunhofer-Gesellschaft. "With our practice-oriented research and close collaboration with industry, academia, and political partners, we lay

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the foundation not only for developing cutting-edge technologies but also for bringing them into industrial application. APECS is an example how to connect research with business – it underscores how close cooperation with ministries and other partners can secure Europe´s position in the global microelectronics market."

Innovation where European industries need it the most

The *APECS* pilot line will play a key role in supporting European microelectronics by developing new system integration technologies and unlocking new functionalities within the system-technology co-optimization (STCO) approach. This will enable European companies to develop advanced products, even in low quantities, at competitive costs. By providing a wide range of technologies on a single platform, *APECS* is positioned to become Europe's leading hub for the development of advanced packaging and heterogeneous integration.

APECS will be a key driver of collaboration among European RTOs, industry and academia, fostering a lively innovation ecosystem. Customers will benefit from a single point of contact to the *APECS* pilot line. *APECS* will cover end-to-end design and pilot production capabilities and accelerate progress from cutting-edge research to practical, scalable manufacturing solutions.

Furthermore, *APECS* will play a pivotal role in Europe's transition towards a carbon-neutral and circular economy through its promotion on eco-design and green manufacturing initiatives.

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Boosting Innovation through strong multilevel Collaboration

The *APECS* pilot line builds on the structures established by the Research Fab Microelectronics Germany (FMD). In Germany, twelve institutes from the Fraunhofer Group for Microelectronics and the two Leibniz institutes FBH and IHP participate in APECS. The work is led by the central office in Berlin.

Prof. Albert Heuberger, spokesman of the Fraunhofer Group for Microelectronics and chairman of the FMD, emphasizes: "The success of the EU Chips Act relies on strong partnerships. For years, the FMD has successfully combined the strengths of decentralized research institutions with the collaborative potential of a centralized microelectronics hub. This clearly illustrates how *APECS* is set to become a long-term accessible pilot line for all European stakeholders across the entire value chain. Together with the other EU Chips Act pilot lines, *APECS* will be a crucial component for heterogeneous integration and advanced packaging of the envisioned pan-European pilot line facility – and thus an indispensable instrument of EU Chips Act."

The *APECS* consortium brings together the technological competences, infrastructure, and know-how of ten partners from eight European countries: Germany (Fraunhofer-Gesellschaft as coordinator, FBH, IHP), Austria (TU Graz), Finland (VTT), Belgium (imec), France (CEA-Leti), Greece (FORTH), Spain (IMB-CNM, CSIC) and Portugal (INL). APECS is coordinated by the Fraunhofer-Gesellschaft and implemented by the Research Fab Microelectronics Germany (FMD).

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About Research Fab Microelectronics Germany (FMD)

As a cooperation between the Fraunhofer Group for Microelectronics and the Leibniz Institutes FBH and IHP, the Research Fab Microelectronics Germany (FMD) is the central point of contact for all issues concerning research and development in the field of micro and nanoelectronics in Germany and Europe. As a one-stop shop, FMD has been combining scientific excellence, application-oriented technologies and system solutions of the 13 cooperating institutes from the Fraunhofer-Gesellschaft and Leibniz Association into a customer-specific offering since 2017. With more than 4,900 employees and a diversity of expertise and infrastructure, the virtual umbrella organization of FMD is the largest association of its kind in Europe. www.forschungsfabrik-mikroelektronik.de/en

*About Heterogeneous Integration

Semiconductor research and development is at the core of current technological (r)evolutions, ranging from artificial intelligence and high-performance computing, modern defense systems to robotics, power electronics, wireless communication, e-health care, quantum technologies, and more. Such future electronic systems will require more and more functions that cannot be provided by a single chip, even if advanced system-on-chip (SoC) concepts are used. Heterogeneous integration will go beyond current system-in-package (SiP) approaches. This concept of true heterogeneous integration is extremely important for next-generation devices based on future CMOS nodes, SiGe, SiC, III/Vs such as GaAs or GaN and all different types of microelectromechanical systems (MEMS).

**About Chiplets

For conventional approaches, the amount of data to be stored is too big, the data transfer rates are too low, the available computational power is limiting, and the energy consumption, as well as the heat production of general-purpose computer processing units (CPUs) are too high. In addition, the increasingly higher costs for further node miniaturization in the IC manufacturing process will also promote the interconnection of so called chiplets. This means that intellectual property (IP) blocks made in different technology nodes will be combined on an active interposer to reduce cost by increasing the production yield (smaller chips) and reuse across applications. This will also touch upon environmental properties of electronics in terms of resource efficiency, critical raw materials, modularity and re-usability of design blocks.

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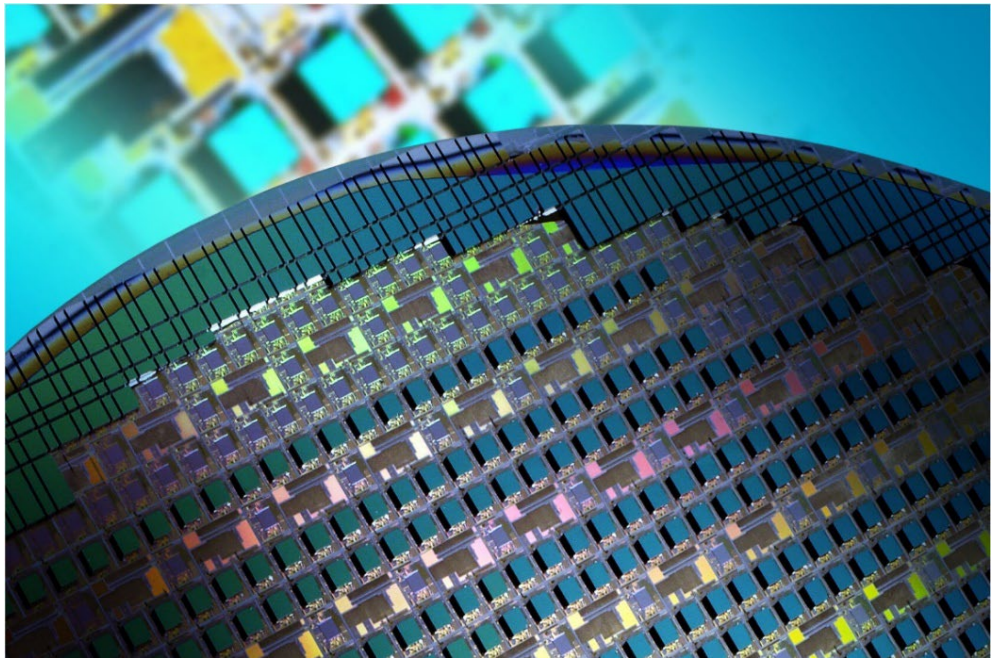
Within the framework of the APECS pilot line will be possible to further expand the R&D infrastructure for semiconductor technologies and applications in the coming years. © loewn | Bernhard Wolf



Post-CMOS pressure sensor chiplets with wafer level packaging before dicing. © Fraunhofer ISIT

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